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Display panel having energy recovery system

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Display panel having energy recovery system

Description of prior art

The invention relates to a flat panel display apparatus comprising plasma discharge cells having sustain electrodes and scan electrodes, a drive circuit having a circuit for providing data to the discharge cells and an energy recovery circuit. The invention also relates to a method of recovering energy in a flat panel display having sustain electrodes and scan electrodes and a drive circuit.

The invention applies particularly to AC plasma display panels (PDPs) used for personal computers, television sets, etc.

In a PDP, each row of the matrix is defined by two electrodes: a scan electrode and a sustain electrode. A cell is defined by one row (two electrodes) and a column electrode.

To show a picture on such a display, a sequence of three driving modes is applied for each sub-frame:

- An erase mode, in which old data in the cells is 'erased', so the next (sub)frame can be loaded.
- An addressing mode, in which the data of the (sub) frame to be shown is written into the cells.
- A sustain mode, in which light (and thus the picture) is generated. All cells are sustained at the same time.

The data is written in subfields to generate grey levels.

Such display devices often comprise an energy-recovery system for recovery of energy.

In such devices, energy recovery can be applied during sustaining (in the direction usually called the row direction) as well as during addressing (thus in the direction usually called the column direction) to reduce the power consumption of the panel. The advantages of energy recovery for the column drivers (i.e. parts of the driving circuit which drive the columns) are a decrease in the power consumption and electromagnetic radiation.

It is an object of the invention to provide a display device as described in the first paragraph in which energy recovery during addressing is improved.

To this end a display device in accordance with the invention is characterized in that the data is arranged in subfields and the means for activating the energy recovery circuit are for activating the energy recovery circuit only for a part of the total number of subfields.

The invention is based on the insight that energy recovery for the column drivers is beneficial when the data on the columns changes value (1 to zero or zero to 1, or more in general active to non-active and vice-versa) while it is unfavorable when the data has to remain high. An apparent solution would be to only apply energy recovery for the columns where the data changes value. However, this is not possible because many if not all columns are connected to the same power cable and energy recovery system. Therefore, energy recovery can only be applied for a group of (or all) columns or for no column at all.

PDPs are conventionally driven by the so-called subfield driving scheme to create grey levels. In a device in accordance with the invention energy recovery for the column drivers is applied only for a limited number of subfields. For some of the subfields, so the inventors have found, energy recovery may in fact cost energy. Activating the energy recovery circuit for such subfields is disadvantageous.

In preferred embodiments the part of the sub fields during which in operation the energy recovery circuit is activated has on average a lower subfield weight than the rest of the sub-fields.

Subfields with a low weight will have a very low data correlation. Consequently, the data values will change often and energy recovery is desirable. On the other hand, subfields with a high weight will have a high data correlation. Thus, the data will remain high (or low) often and energy recovery is not desirable. By using this invention, energy recovery is only applied for part of the subfields (a part having relatively higher weights). Over all, this will result in a better power consumption and EMI reduction. Preferably the said part of the sub fields are all lower in weight or equal in weight than the sub fields for which in operation the energy recovery circuit is activated.

In a preferred embodiment the display apparatus comprises a discriminator having means for choosing, on the basis of the data to be displayed, the part of the subfields during which the energy recovery circuit is activated.

These and other objects of the invention are apparent from and will be elucidated with reference to the embodiments described hereinafter.

Short description of the drawings

In the drawings:

Fig. 1 is a cross-sectional view of a pixel of a PDP device

Fig. 2 schematically illustrates a circuit for driving a PDP of a surface-discharge type in a sub-field mode as known from the prior-art.

Fig. 3 illustrates voltage waveforms between scan electrodes and sustain electrodes of the known PDP.

Fig. 4 further illustrates the layout of pixels in a plasma display panel

Figs. 5 to 6e illustrate an energy recovery scheme for recovering energy in the sustain phase.

Figs. 7 to 8d illustrate an energy recovery scheme for recovering energy in the address phase.

Figure 9 shows in a graphical form the energy recovery in the address phase as a function of sub-field number for a video image.

Figure 10 shows in a graphical form the energy recovery in the address phase as a function of sub-field number for a data-graphics image.

The Figures are schematic and not drawn on scale. Generally, identical components are denoted by the same reference numerals in the Figures.

Detailed description of preferred embodiments

The prior-art pixel shown in Fig. 1 produces an image in the following steps.

Fig. 1 illustrates the structure of a pixel (discharge cell). The pixel comprises a back substrate structure 1 and a front structure 2, and a partition wall 3 which spaces the back structure 1 from the front structure 2. Discharge gas 4 such as helium, neon, xenon or a gaseous mixture thereof fills the space between the back structure 1 and the front structure 2. The discharge gas generates ultra-violet light during discharging. The back structure 1 includes a transparent glass plate 1a and a data electrode 1b is formed on the transparent glass plate 1a. The data electrode 1b is covered with a dielectric layer 1c, and a phosphor layer 1d is laminated on the dielectric layer 1c. The ultra-violet light is radiated onto the phosphor layer 1d, and the phosphor layer 1d converts the ultra-violet light into visible light. The visible light is indicated by arrow AR1. The front substrate 2 includes a transparent glass plate 2a, and a scan electrode 2b, 2d and a sustain electrode 2c, 2e are formed on the

transparent glass plate 2a. The scan electrode 2b, 2d and the sustain electrode 2c, 2e extend perpendicularly to the data electrode 1b. These electrodes 2b, 2c, 2d and 2e are covered with a dielectric layer 2f, and the dielectric layer 2f may be covered by a protective layer 2g. The protective layer 2g is for instance formed of magnesium oxide and protects the dielectric layer 2f from the discharge. An initial potential larger than the discharging threshold is applied between a scan electrode 2b and a data electrode 1b. Discharging takes place between them. Positive charge and negative charge are attracted towards the dielectric layers 2f/1c over the scan electrode 2b and the data electrode 1b and are accumulated thereon as wall charges. The wall charges produce potential barriers and gradually decrease the effective potential. Therefore, the discharge is stopped after some time. Thereafter, a sustain pulse is applied between the scan electrodes 2b and the sustain electrodes 2c which pulse is identical in polarity to the wall potential. Therefore, the wall potential is superimposed on the sustain pulse. Because of the superimposition the effective potential exceeds the discharging threshold and a discharge is initiated. Thus, while the sustain pulse is being applied between the scan electrodes 2b and the sustain electrodes 2c, the sustain discharge is initiated and continued. This is the memory function of the device. This process occurs in all pixels at the same time.

When an erase pulse is applied between the scan electrodes 2b and the sustain electrodes 2c, the wall potential is cancelled, and the sustain discharge is stopped. The erase pulse has a wide pulse width.

Figure 2 schematically illustrates a circuit for driving a PDP of a surface-discharge type in a sub-field mode as known from the prior art. Two glass panels (not shown) are arranged opposite to each other. Data electrodes D are arranged on one of the glass panels. Pairs of scan electrodes Sc and sustain electrodes Su are arranged on the other glass panel. The scan electrodes Sc are aligned with the sustain electrodes Su, and the pairs of scan and sustain electrodes Sc, Su are perpendicular with respect to the data electrodes D. Display elements (for example, plasma cells or pixels C) are formed at the crosspoints of the data electrodes and the pairs of scan and sustain electrodes Sc, Su. A timing generator 21 receives display information Pi to be displayed on the PDP. The timing generator 21 divides a field period Tf of the display information Pi into a predetermined number of consecutive sub-field periods Tsf as shown in Fig. 3. A sub-field period Tsf comprises an address period or prime period Tp and a display or sustain period Ts. During an address period Tp, a scan driver 22 supplies pulses to the scan electrodes Sc, and a data driver 23 supplies data di to the data electrodes D to write the data di to the display elements C associated with the selected scan

electrode Sc. In this way the display elements C associated with the selected scan electrode Sc are preconditioned. A sustain driver 26 drives the sustain electrodes Su. During an address period Tp, the sustain driver 26 supplies a fixed potential. During a display period Ts, a sustain pulse generator 25 generates sustain pulses Sp which are supplied to the display elements C via the scan driver 22 and the sustain driver 26. The display elements, which are preconditioned during the address period Tp to produce light during the display period Ts, produce an amount of light depending on a number or a frequency of sustain pulses Sp. It is also possible to supply the sustain pulses Sp to either the scan driver 22 or the sustain driver 26. It is also possible to supply the sustain pulses Sp to the data driver 23 or both to the scan driver 22 or to the sustain driver 26 and the data driver 23.

The timing generator 21 further associates a fixed order of weight factors Wf with the sub-field periods Sf in every field period Tf. The sustain generator 25 is coupled to the timing generator to supply a number or a frequency of sustain pulses Sp in conformance with the weight factors Wf such that an amount of light generated by the preconditioned display element C corresponds to the weight factor Wf. A sub-field data generator 24 performs an operation on the display information Pi such that the data di is in conformance with the weight factors Wf.

When regarding a complete panel, the sustain electrodes Sc are often interconnected for all rows of the PDP panel. The scan electrodes Sc are connected to row ICs and scanned during the addressing or priming phase. The column electrodes D are operated by column ICs and the plasma cells C are operated in three modes:

1. Erase mode. Before each sub-field is primed, all plasma cells C are erased at the same time. This is done by first driving the plasma cells C into a conducting state and then removing all charge built up in the cells C.

2. Prime mode. Plasma cells C are conditioned such that they will be in an on or off state during the sustain mode. Since a plasma cell C can only be fully on or off, several prime phases are required to write all bits of a luminance value. Plasma cells C are selected on a row-at-a-time basis and the voltage levels on the columns will determine the on/off condition of the cells. If a luminance value is represented in 9 bits, then also 9 sub-fields are defined within a field. Different examples of sub-field distributions are possible.

3. Sustain mode. An alternating voltage is applied to scan and sustain electrodes Sc, Su of all rows at the same time. The column voltage is mainly at a high voltage potential. The plasma cells or pixels C primed to be in the on state, will light up. The weight of an individual luminance bit will determine the number of light pulses during sustain.

Fig. 3 shows voltage waveforms between scan electrodes Sc and sustain electrodes Su of a PDP. Since there are three modes, the corresponding time sequence is indicated as Te,bx (erase mode for bit-x sub-field), Tp,bx (prime mode for bit-x subfield) and Ts,bx (sustain mode for bit-x subfield). The different subfields are indicated by SF1, SF2 etc. In this example there are six subfields (SF1 to SF6) within the field T_f. The sub field distribution is 4/16/32/8/2/1

Fig. 4 further illustrates the layout of pixels C in a plasma display panel Pa. The pixels are identical in structure to the pixel shown in Figure 1 and form a display area. The pixels are arranged in j rows and k columns, and a small box stands for each pixel in Figure 4. Scan electrodes (Sci) and sustain electrodes (Sui) extend in the direction of the rows, and the scan electrodes are paired with the sustain electrodes respectively. The pairs of scanning/sustain electrodes are associated with the rows of pixels respectively Data electrodes (Di) extend in the direction of columns, and are associated with the columns of pixels, respectively.

In energy recovery systems, energy recovery circuits are usually arranged between the scanning and sustain electrodes or between each group of electrodes and buffer capacitors. As a consequence, current leads which must be capable of carrying large currents (which can be as large as 100 amp) run over the length of the device usually along the rear side, or extra components (the buffer capacitors) are needed.

By means of example a recovery systems for recovering energy during the sustain phase is schematically shown in Figures 5, 6a to 6e.

Because of the mainly capacitive character of a PDP (Plasma Display Panel), with a proper energy recovery circuit, blind power dissipation and EMI can be strongly improved. In the Figures 5 and 6a to 6c an energy recovery circuit is arranged between the scanning and common 'row electrodes' or between a group of these electrodes. In Figure 5, the so called Weber energy recovery topology is connected to the 'row electrodes' of a PDP. In the Figures 5 and 6 the scan side of the panel is denoted by Sc, the common side by Co. In this recovery system buffer capacitors Cbuffer are used at both sides of the panel to store energy and re-use it. The different switches are denoted s1 and s2 (for the scan side), c1 and c2 (for the common side) and e1 to e4 for switches for the energy recovery circuits. The panel capacitance is indicated by Cpanel. Figure 5 shows schematically the panel with energy recovery circuits at both sides of the panel. With The Weber energy recovery topology, the voltage over the panel capacitor is inverted in two steps. These steps are shown in Figures 6a to 6d, while in Fig. 6e the currents and sustain voltages are indicated as a function of time,

i.e. within the different periods indicated in Figures a to d. Finally at the bottom of the lowest graph it is indicated which switches are activated in which periods. In Figure 6b the scan-side of the panel is discharged and stored in a buffer capacitor Cbuffer. The arrow in this Figure 6b illustrates the recovery current Irecover1. Now the common-side of the panel capacitance must be charged again, which is done in Figure 6c. Charge is transferred from panel capacitance Cpanel to buffer capacitances Cbuffer and vice-versa. Instead of throwing away the energy during discharging, the energy is therefore recovered via the buffer capacitances.

Figs. 7 to 8d illustrate an energy recovery scheme for recovering energy in the address phase.

Also in addressing the 'column electrodes', a large capacitive load has to be driven. The idea of storing and re-using energy as is done for the row capacitances, may also be implemented with respect to the stored energy in the column capacitances (and hereby improving the power dissipation and EMI). Things are a bit different, still with the resonant circuitry based on the Weber topology energy in the column capacitances will be stored and re-used again. A principle schematic of energy recovery for the column electrodes (in the addressing phase) of a PDP is shown in Figure 7. To drive the column electrodes is done by means of data driver ICs. For simplicity, only one column is driven by one output stage (denoted by switches sIC1 and sIC2) of a data driver IC. In practical each column can be pulled to the 'VDH node' (see Figure 8) or 'ground' by similar sIC 1 and sIC2 switches in the data driver ICs. Compared to Figure 5, in this case only a single energy recovery circuitry is present and therefore also one buffer capacitor Cbuffer. The different switches in the circuitry are denoted s I (to supply the data driver ICs with Vaddress) and e3 and e4 for recovering energy. With this circuitry, the supply voltage 'VDH' for the data driver ICs is controlled in a resonant way.

A complete sequence of storing and re-using stored energy in the columns is shown in the Figures 8a to 8c. In Figure 8d the currents and voltages are indicated as a function of time, i.e. within the different periods indicated in Figures 8a to 8c. Finally at the bottom of the lowest graph it is indicated which switches are activated in which periods. In Figure 8a, the supply pin (VDH) of the data driver ICs are pulled to a fixed voltage source (typically 6OV) by means of switch sl. Hereby, the data driver ICs are supplied with a stable voltage which is essential for properly addressing columns. The addressing of the correct columns for the scanned row, is done by the control lines to the data driver ICs. Via the switches sIC1 and sIC2 a column is pulled to the address voltage VDH or to ground.

Columns which are pulled to VDH are said to be addressed and columns pulled to ground are said not to be addressed.

After the appropriate columns are addressed, switch s1 is deactivated and the switches in the data driver ICs (sIC 1 and sIC2) are set in their 'high-impedant' mode. Now, the columns are floating while the charge in the addressed columns remains (via the capacitive behavior of a column). With switch e4 and the parasitic diodes in parallel with switches sIC1 (Figure 8b), an inductor Lrecover is connected in series with the column capacitances. A sine-wave current will start to flow, and the voltage over the charged columns decreases in a cosine way. The flowing current and the column voltage during 'energy storing' are shown next to Figure 8b. In this circuit use is made of a half-period of the resonance phenomenon (determined by Ccolumns and Lrecover). When half a sine-wave is completed, the current (Istore) passes a zero-crossing. By inserting a diode in series with switch e4, the current is prohibited to go negative. At this point the voltage over the column capacitances has reached its minimum.

Simultaneously with storing energy, data corresponding with the next row to address is transferred to the driver ICs. As the half sine-wave for storing energy is completed, this 'new' data is set to activate the appropriate sIC 1 and sIC2 switches. Hereby the correct columns are connected to the VDH node, and switch e3 is activated (Figure 8c). Of those columns where switch sIC 1 is activated, the stored energy in the buffer capacitor is transferred back to the panel. In the opposite direction a sine-wave current will start to flow, and the voltage over the selected columns increases in a cosine way. This reuse of the stored energy is shown in Figure 8d. Again when half a sine-wave is completed, the current (Ireuse) passes a zero crossing and is blocked to flow back by the diode set in series with switch e3. Inevitable losses are present in the resonance loop, and therefore switch sl is activated to pull the VDH supply line for the data driver ICs to Vaddress. Now, the driver ICs are supplied with a stable voltage and the appropriate columns are properly addressed. With this, one full period of addressing columns, storing energy and regaining energy has completed.

For improved operation of the circuit, quite a large buffer capacitor is preferred. If this is the case, the voltage rise and fall over the buffer capacitor (during storing and regaining energy) will be negligible and will stabilize at half the address voltage (which is typically 30V).

The invention is based on the insight that energy recovery for the column drivers is beneficial when the data on the columns changes value (active to non-active or vice-versa) while it is unfavorable when the data has to remain high. PDPs are driven by the

so-called subfield driving scheme to create grey levels. The invention is now that the energy recovery for the column drivers is applied only for a limited number of subfields. Subfields with a low value will have a very low data correlation. Consequently, the data values will change often and energy recovery is desirable. On the other hand, subfields with a high value will have a high data correlation. Thus, the data will remain high (or low) often and energy recovery is not desirable. By using this invention, energy recovery is only applied for subfields if it is desirable. Over all, this will result in a lower power consumption and EMI reduction. The beneficial effect of the invention is illustrated by the results of calculations. For the calculations, it is assumed that interlaced addressing, i.e. an addressing scheme in which first the odd rows and then the even rows are addressed whereafter the whole image is sustained, is used. Please note that this will decrease the data correlation (because two temporal consecutive rows are spatially larger separated). The calculations are actually quite simple:

- First, for each column (R,G,B) and each subfield in the picture, all transitions from zero to one and one to zero (or more generally active to non-active) are counted. This is a Figure for the power consumption without using energy recovery.
- Second, for each pixel (R,G,B) and each subfield of the picture, the number of times that a small trailing edge in voltage is present is counted (see Figure 8, V versus t part, in which the voltage after Ire-use phase is slightly below the 'normal addressing voltage, this edge accounts for the losses during the recovery loop). This number is multiplied by the loss-factor during energy recovery (which is assumed to be 30%). Now, the calculated value is a Figure for the power consumption when energy recovery is applied.

When this is done for an image with 8 binary weighted subfields (weights: 1/2/4/8/16/32/64/128), this results in a graph as shown in Figure 9. The bold line represents the results of the calculations without energy recovery and the dotted line the results with energy recovery. This graph shows the result for video information. Clearly, there is a break-even point: using energy recovery for the low weighted subfields gives a significant reduction and energy recovery for the higher weighted subfields results in an increase in the dissipated power. According to the invention, energy recovery in the column direction should only be used for the 4 or 5 subfields with the lowest values.

Identical calculations may be performed for 16 different pictures. The results are shown in Table 1. The second column indicates the relative reduction of power consumption if energy recovery is applied for all subfields compared to the initial situation without applying energy recovery. The third column indicates the reduction when the

invention of subfield selective energy recovery is used, compared to the situation without energy recovery. Energy recovery for all subfields gives a 20% reduction while the invention gives a 27% reduction in power dissipation.

Table 1: Results for 16 different images

subfield improvement distribution	improvement by using ER for all subfields	improvement by using subfield selective ER	using row selective ER
binary subfields	+20%	+27%	+28%
duplicated subfields	-20%	+17%	+19%

In the above-described calculations, binary weighted subfields are used. However, there are more possible ways of distribution of the sub-fields. Therefore, identical calculations are done for Duplicated Subfields (weights 12/8/4/2/1/4/8/12). This is a subfield distribution that decreases the perception of motion artifacts, and it is implemented in many commercial available panels (for example FHP). For an example of a description of a duplicated subfield addressing scheme reference is made to ASIA Display'96, Part S-19-3, 'Improvement of Video Image Quality in AC Plasma Display Panels by Suppressing the Unfavorable Coloration Effect with Sufficient Gray Shades Capability' by T. Makino, A. Mochizuki et al., which reference hereby incorporated. The results of the calculations are also shown in table 1, under 'duplicated subfields', and at first, they may seem somewhat surprising. If energy recovery is applied for all subfields, the power consumption will increase! This can be explained by the duplication of the subfields. If a duplicated subfield is turned on for a certain pixel, the chance is large that it is also turned on for the next addressed row (if interlaced addressing is used). If energy recovery is now applied according to the invention, the power consumption will decrease by 17%, which is a significant reduction.

The examples so far relate to display of video information. Figure 10 illustrates the results for data graphics (i.e. for instance black text on a white background). For such types of images because of the much smaller number of changes in data, the 'break-even point' lies at a relatively lower subfield and only for the first two subfields energy recovery is used. Use of a discriminator may be preferred in such embodiments where it is useful and possible to make a distinction between the type of information displayed (video or data graphics) and then selecting the proper number of subfields.

In another embodiment of the invention discrimination is not done per subfield, but per row. For each row must now be calculated if energy recovery is desirable or not. This can be done with the same calculations, but they are now done per row instead of per subfield. The last column in Table 1 shows the results for row-selective energy recovery. The reduction in power consumption is somewhat larger than for subfield selective energy recovery. However, this embodiment of the invention requires a calculation which complicates the design of the apparatus as will be shown below.

Now the only remaining question is for which subfields the energy recovery should be set active and for which it should be set inactive. A straightforward way of doing this is simply doing the calculations as is described in the last section. However, this would have to be done for each subfield, and the total number of operations will be very large. This is also true when row selective energy recovery is used. The total number of calculations per second equals: #rows * #dots * 3 (with and without ER and a comparison) * #frames. Furthermore, a line memory is required. If a VGA display is used at 50Hz, this will result in 480*850*3*50*3 = 180 million operations per second!

An alternative solution is shown in Table 2. The 3rd column shows the relative reduction of power consumption when the invention is used for a fixed number of subfields. Surprisingly, the difference with the situation when the optimal number of subfields is chosen is very small. By using a fixed number of subfields, almost the entire gain can be obtained without the need for a huge number of operations per second.

Table 2: Results for a fixed number of subfields

subfield	improvement with subfield selective ER acc. to Table Is	improvement by using a fixed # of subfields	# of subfields that do not apply ER
binary subfields	+27%	+26%	3
duplicated subfields	+17%	+17%	6

As we have seen, this fixed number of subfields that do not apply ER depends on the subfields distribution (binary weighted subfields, duplicated subfields). Furthermore, it also depends on the efficiency in which energy is recovered. Other variables that can be used are the display- or subfield-load. If the display load is high, it is likely that the data correlation is higher, and energy recovery should be applied for less subfields. These variables usually are

measured by a digital board so they can simply be reused to control the energy recovery circuit. Finally, the last variable is the display mode. The pictures that were used in the calculations are all video images. For data graphics, the data correlation is much higher, and energy recovery shall probable be beneficial for less subfields. Al such parameters may be fed or calculated by a discriminator. However, they are relatively simple to calculate and thus do not require extensive calculating power.

Within the overall framework of the invention the choice of the number of subfields, or the subfields themselves during which the energy recovery circuit is, in operation, activated may be different from embodiment to embodiment. In a simple, yet already relatively very advantageous embodiment the number of subfields during which the energy recovery circuit is activated is fixed, for instance the two, three or four lowest weight sub fields. The choice of the subfields may be dependent on the way in which the data is arranged, i.e. the distribution of subfields.

In more elaborate display apparatuses a discriminator is used which, based on the data to be displayed, calculates the advantages/disadvantages of energy recovery (or has data providing the relation between advantages/disadvantages and a certain parameter) and chooses the subfields or the number of subfields during which the energy recovery circuit is activated or de-activated. One such parameter is, as described above, the panel load. This is an easily retrievable parameter. A discriminator may be any piece of hardware and/or software able to calculate or determine the effects and effecting a choice. Using such a discriminator it is also possible to make the calculation per row and to activate or deactivate the energy recovery circuit per row displayed. Figure 10 for instance illustrates the results for a data graphics (i.e. for instance black text on a white background). For such types of images because of the much smaller number of changes in data, the 'break-even point lies at a relatively lower subfield and only for the first two subfields energy recovery is used. A discriminator can decide given the nature or parameters of the image to be displayed for which sub-fields energy recovery is activated.

How many columns are addressed for a particular row is of course dependent on the video content. With this, also the half-period of a resonant cycle is dependent on the video content.

$To=2\pi*SQRT(L_{recover}*n*C_{columns})$

$t_{store}=t_{regain}=Tp/2=\pi*SQRT(L_{recover}*n*C_{columns})$

In this formula, 'n' denotes the number of addressed columns and 'Ccolumns' denotes the capacitance of a single column. If all columns where (or have to be) addressed, the half period resonant time will be maximal (n is maximum). The other extreme is only one column was (or has to be) addressed, then the half period will be minimal (n=l). In contrast with a varying half-period time, activating and deactivating the switches is done with fixed time-intervals. It seems best to set the time intervals of the switches in correspondence with the maximum half-period resonant time. For instance, this time interval for storing (and re-using) energy may be set at 250ns. It is important to realize, that this time will be consumed for each scanned row in each subfield where energy recovery is active!

Without applying 'subfield selective energy recovery for the columns' as much as 2ms is consumed for recovering energy in the addressing phases.

$t_{recover}=n_{rows}*m_{subfields}*(t_{store}+t_{regain})$

$t_{recover}=480*8*500*10^{-9}=2msec$

This extra consumed time in the addressing phases, is subtracted from the sustain phases. Less sustaining time (in this example 2ms) leads to a less bright picture and is considered to be a disadvantage.

Applying the present 'subfield selective energy recovery for the columns' invention, leads to less consumed time by the addressing phases. After all, only for a certain amount of subfields energy recovery is made active. It might be the case that for only the four lowest subfields energy recovery is made active.

$t_{recover}=n_{rows}*m_{ERsubfields}*(t_{store}+t_{regain})$

where $m_{Ersubfields}$ stands for the number of subfields for which energy is recovered (in this case 4) thus.

$t_{recover}=480*4*500*10^{-9}=1msec$

With this example, only 1ms is subtracted from the sustain phases. With more time available in the sustain phases, a brighter picture can be displayed.

It will be clear that the invention is not restricted to the given exemplary embodiment, for instance, in all descriptions thus far, the cells are in the off-state when the addressing phase begins, and all cells that should emit light are made active. The opposite is also possible. In that case, all cells are activated in the erase phase (which is then called the setup phase), and all cells that should not emit light are made inactive during the addressing phase. There is still switching between active and inactive states. Furthermore, there is still a high data correlation for the subfields with a high weight and a low data correlation for the subfields with a low weight. Therefore, the invention is applicable to both kinds of addressing schemes.

In short the invention can be described by:

In a flat panel display apparatus comprising plasma discharge cells having sustain electrodes and scan electrodes, a drive circuit having a circuit for providing data to the discharge cells incorporating an energy recovery circuit and means for activating the energy recovery circuit is provided. The data supplied to the discharge cells is arranged in subfields and the means for activating the energy recovery circuit activate the energy recovery circuit only for a part of the total number of subfields.

It should be noted that the above-mentioned embodiments illustrate rather than limit the invention, and that those skilled in the art will be able to design many alternative embodiments without departing from the scope of the appended claims. In the claims, any reference signs placed between parentheses shall not be construed as limiting the claim. The word "comprising" does not exclude the presence of elements or steps other than those listed in a claim. The word "a" or "an" preceding an element does not exclude the presence of a plurality of such elements. The invention can be implemented by means of hardware comprising several distinct elements, and by means of a suitably programmed computer. In the device claim enumerating several means, several of these means can be embodied by one and the same item of hardware. The mere fact that certain measures are recited in mutually different dependent claims does not indicate that a combination of these measures cannot be used to advantage.

CLAIMS:

1. Flat panel display apparatus comprising plasma discharge cells having sustain electrodes (2c) and scan electrodes (2b), a drive circuit having a circuit for providing data to the discharge cells incorporating an energy recovery circuit and means for activating the energy recovery circuit, characterized in that the data is arranged in subfields and the means for activating the energy recovery circuit are for activating the energy recovery circuit only for a part of the total number of subfields.

2. Flat panel display apparatus according to claim 1, characterized in that said part of the subfields has on average a lower weight than the rest of the sub-fields.

3. Flat panel display apparatus as claimed in claim 2, characterized in that the said part of the subfields are all lower in weight or equal in weight than the sub fields for which in operation the energy recovery circuit is not activated.

4. Flat panel display apparatus according to claim 1, characterized in that the display apparatus comprises a discriminator having means for choosing, on the basis of the data to be displayed, the part of the subfields during which the energy recovery circuit is activated.

5. Flat panel display apparatus according to claim 4, characterized in that the discriminator in operation discriminates depending on the display- and/or subfield-load.

6. Flat panel display apparatus according to claim 1, characterized in that the number of subfields in which energy recovery is applied is fixed.

7. Method for displaying images on a flat panel display apparatus comprising plasma discharge cells having sustain electrodes and scan electrodes, a drive circuit having a circuit for providing date to the discharge cells and an energy recovery circuit and means for activating the energy recovery circuit, characterized in that the data is supplied in subfields

and the means for activating the energy recovery circuit is activated only for a part of the total number of subfields.

ABSTRACT:

In a flat panel display apparatus comprising plasma discharge cells (c) having sustain electrodes (Su) and scan electrodes (Sc), a drive circuit having a circuit (23) for providing data to the discharge cells (c) incorporating an energy recovery circuit and means for activating the energy recovery circuit is provided. The data supplied to the discharge cells (c) is arranged in subfields and the means for activating the energy recovery circuit activate the energy recovery circuit only for a part of the total number of subfields.

Fig. 2

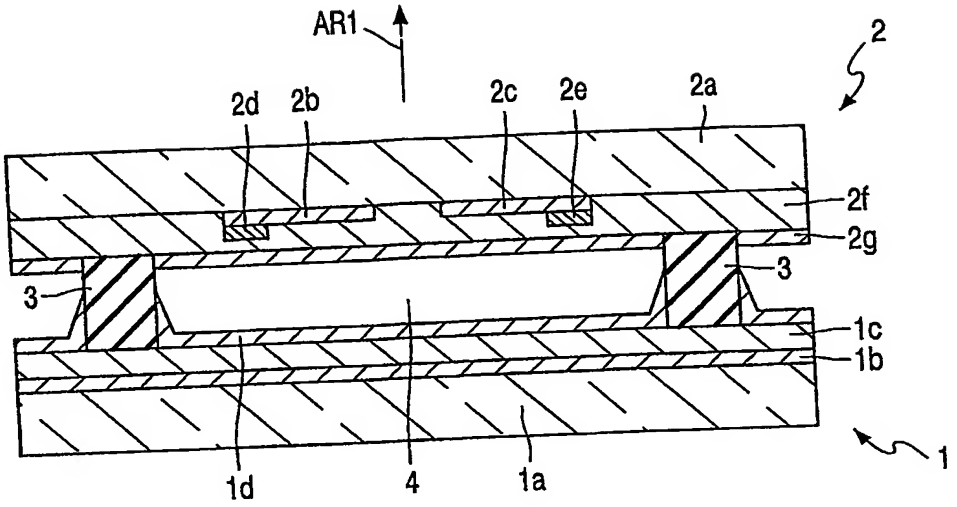
AR1
2
2d
2b
2c
2e
2a
2f
2g
3
3
1c
1b
1d
4
1a
1

FIG. 1

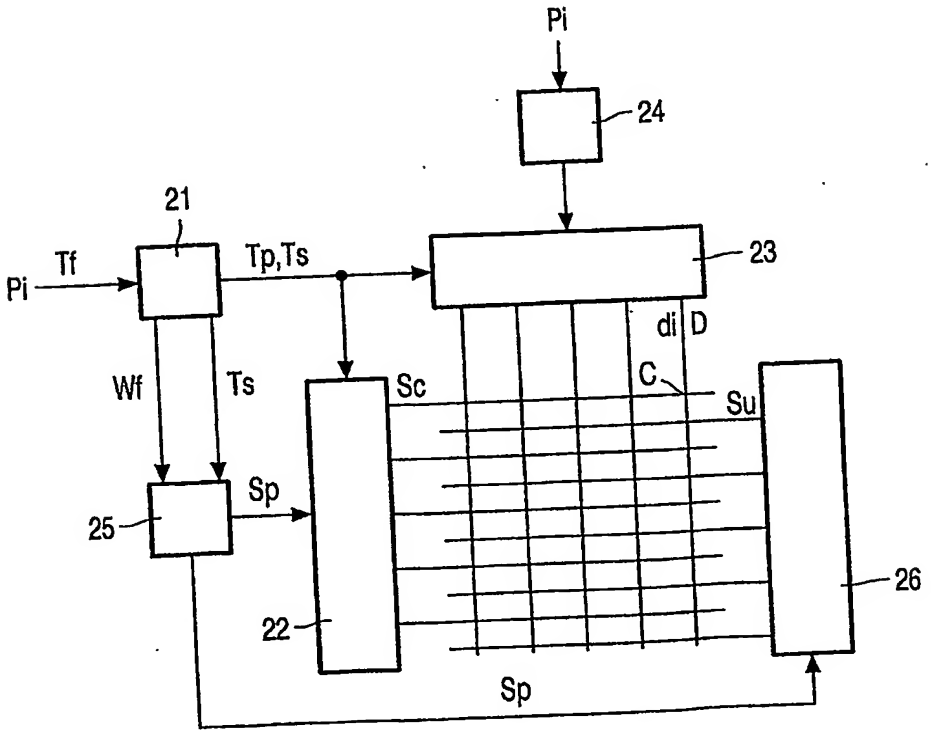
Pi
24
21
Tf
Pi
Tp,Ts
23
di
D
Wf
Ts
Sc
C
Su
Sp
25
26
22
Sp

FIG. 2

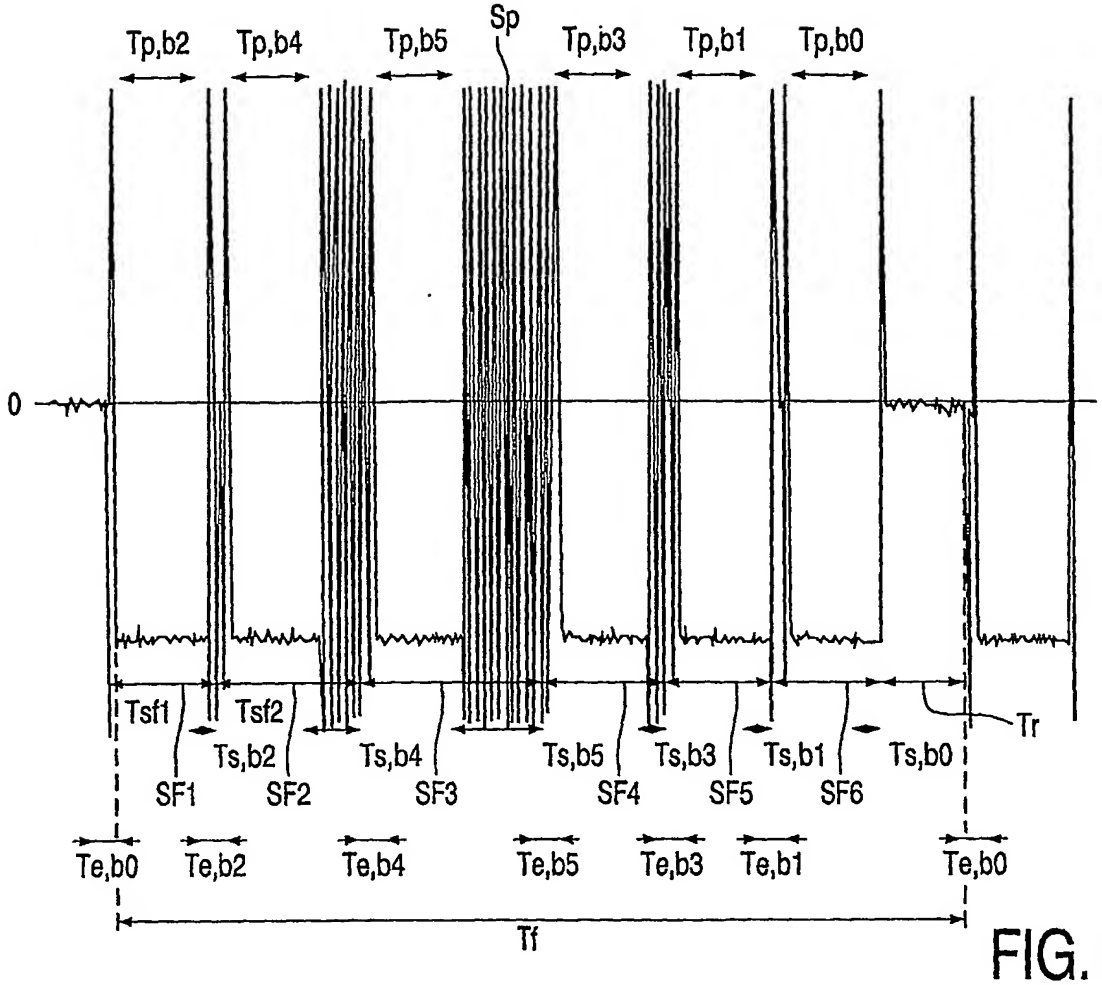
Tp,b2
Tp,b4
Tp,b5
Sp
Tp,b3
Tp,b1
Tp,b0
0
Tsf1
Tsf2
Tr
Ts,b2
Ts,b4
Ts,b5
Ts,b3
Ts,b1
Ts,b0
SF1
SF2
SF3
SF4
SF5
SF6
Te,b0
Te,b2
Te,b4
Te,b5
Te,b3
Te,b1
Te,b0
Tf

FIG. 3

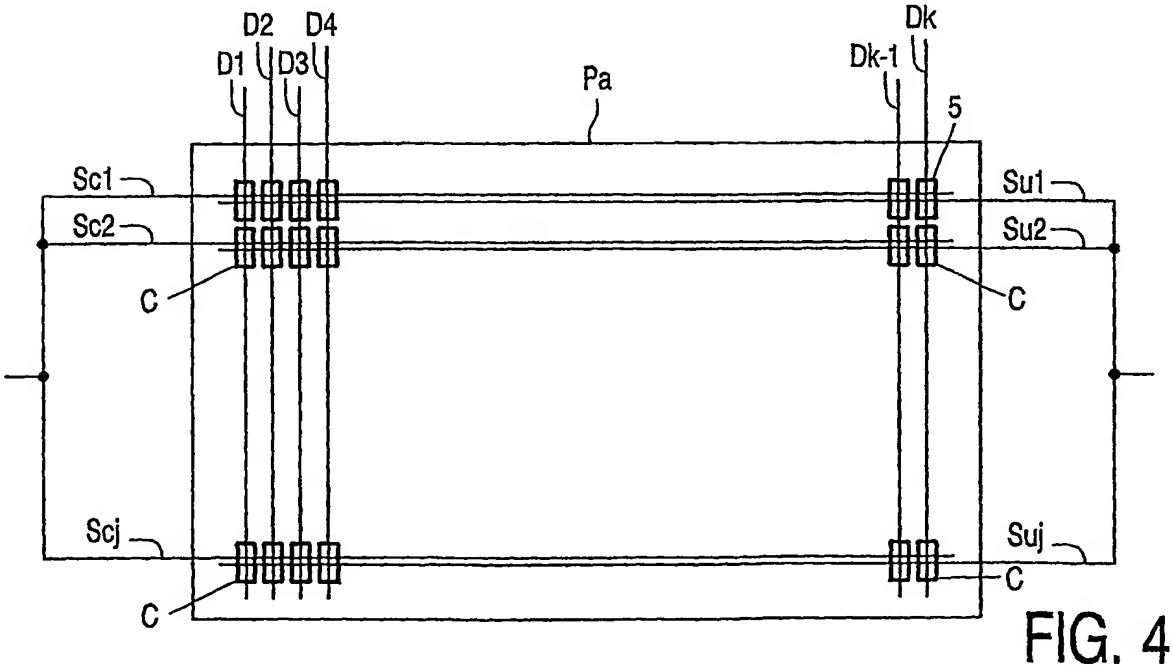
D2
D4
Dk
D1
D3
Dk-1
Pa
5
Sc1
Su1
Sc2
Su2
C
C
Scj
Suj
C
C

FIG. 4

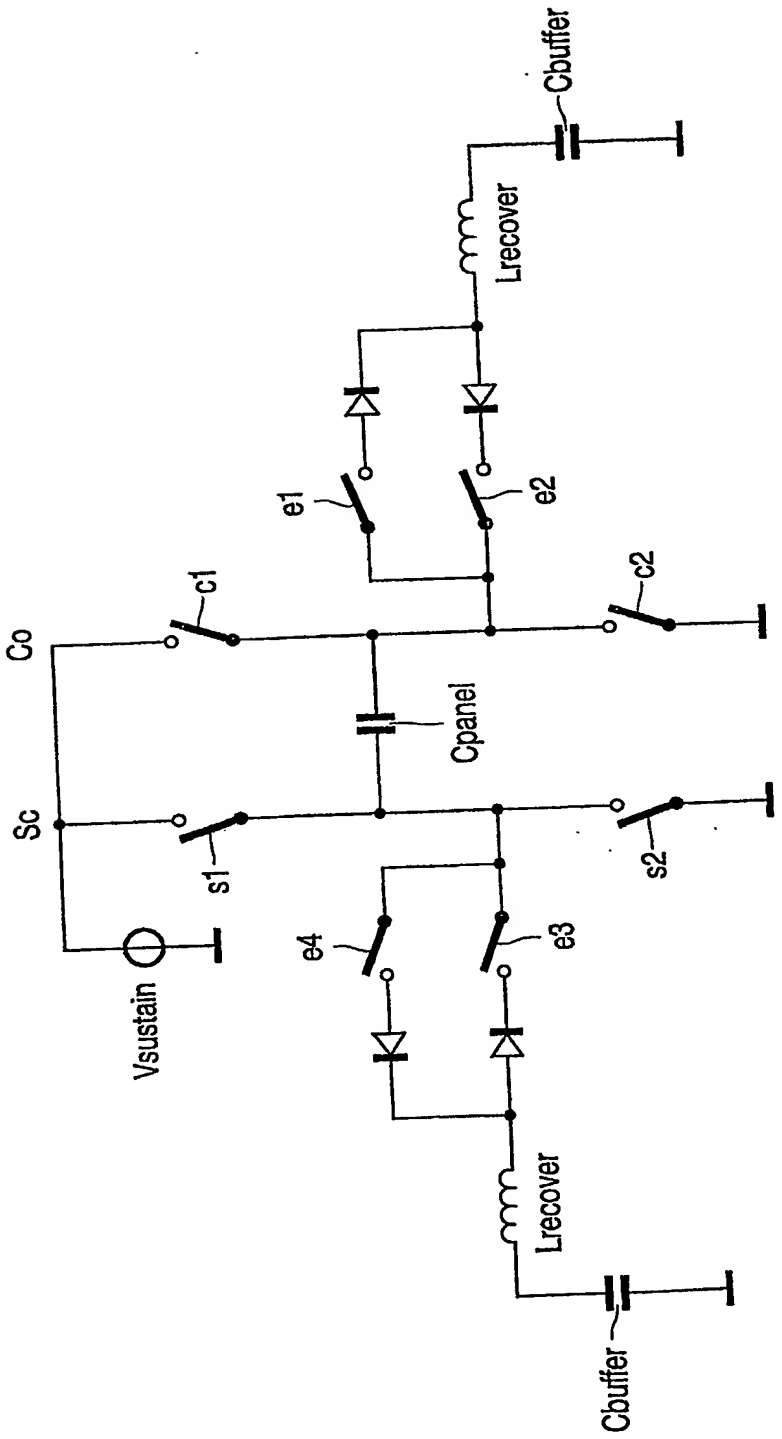
Cbuffer
Lrecover
e1
e2
c1
c2
Co
Cpanel
Sc
s1
s2
e4
e3
Vsustain
Lrecover
Cbuffer

FIG. 5

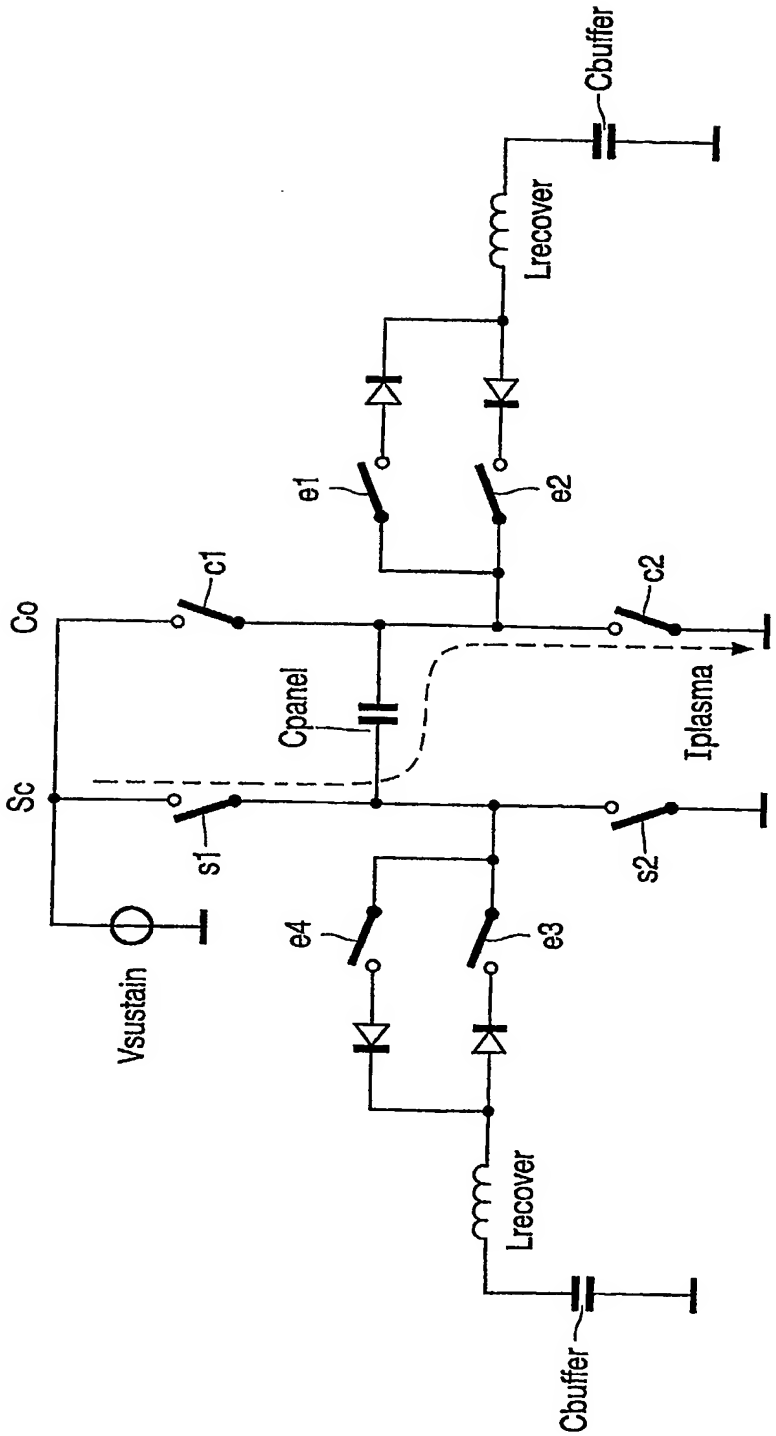
Cbuffer
Lrecover
e1
e2
c1
c2
Co
Cpanel
Iplasma
Sc
s1
s2
e4
e3
Vsustain
Lrecover
Cbuffer

FIG. 6a

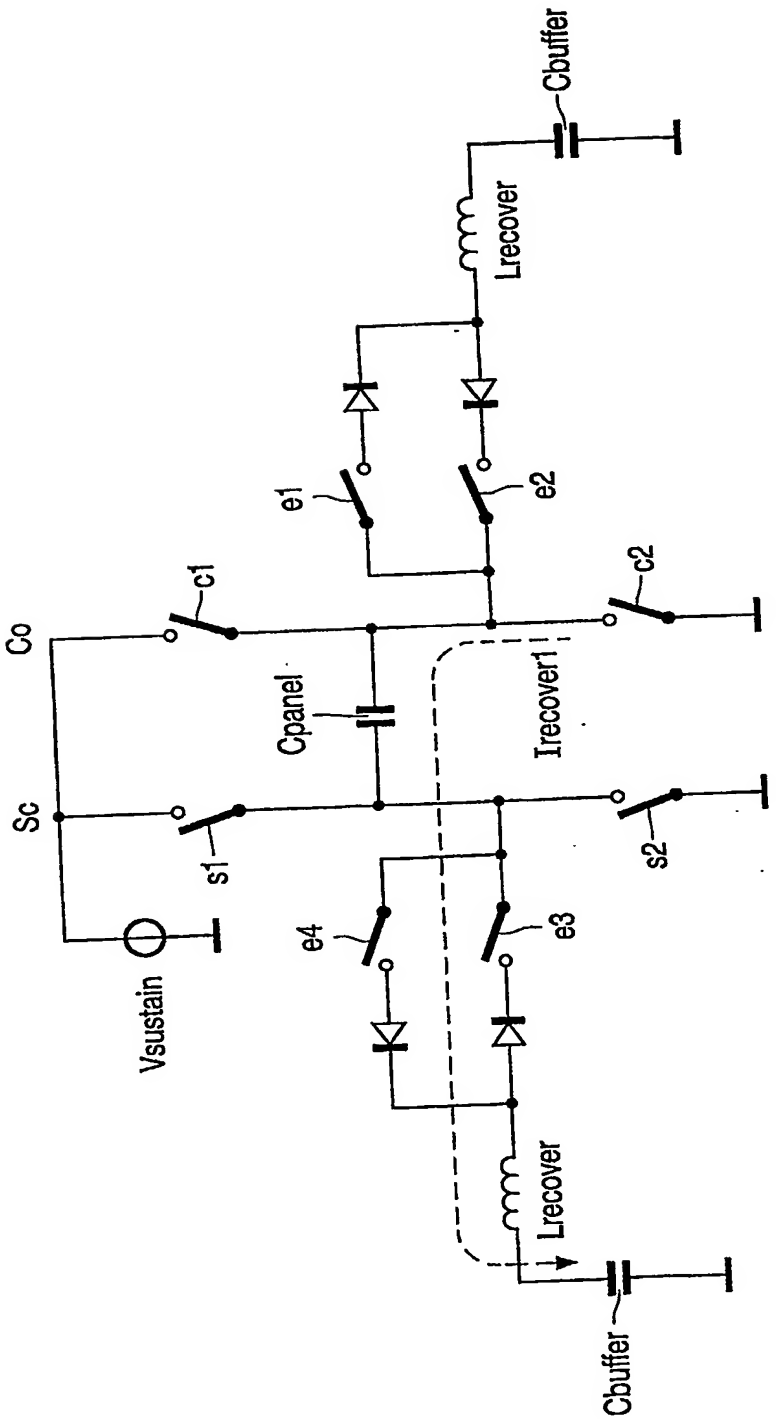
Cbuffer
Lrecover
e1
e2
c1
c2
Co
Cpanel
Irecover1
Sc
s1
s2
e4
e3
Vsustain
Lrecover
Cbuffer

FIG. 6b

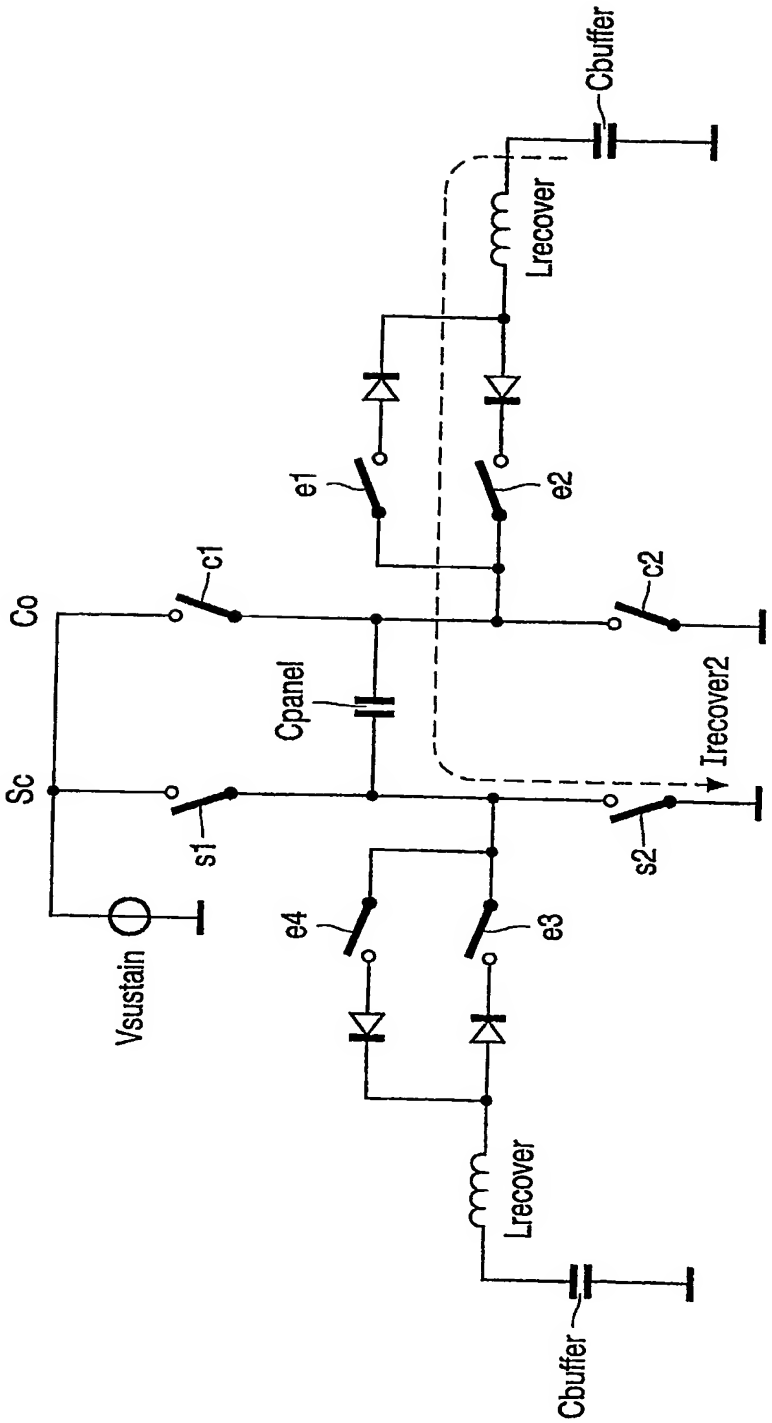
Cbuffer
Lrecover
e1
e2
c1
c2
Co
Cpanel
Irecover2
Sc
s1
s2
e4
e3
Vsustain
Lrecover
Cbuffer

FIG. 6C

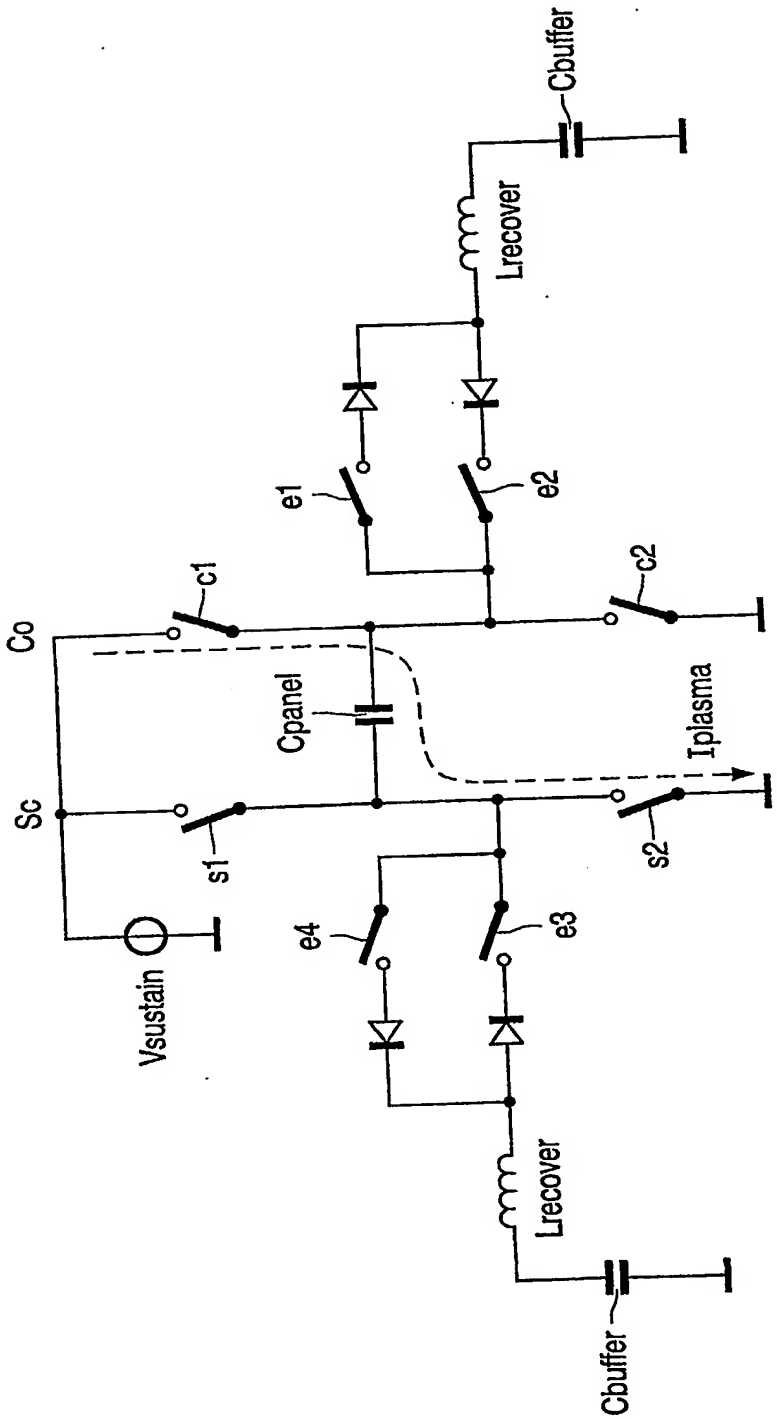
Cbuffer
Lrecover
e1
e2
c1
c2
Co
Cpanel
Iplasma
Sc
s1
s2
e4
e3
Vsustain
Lrecover
Cbuffer

FIG. 6d

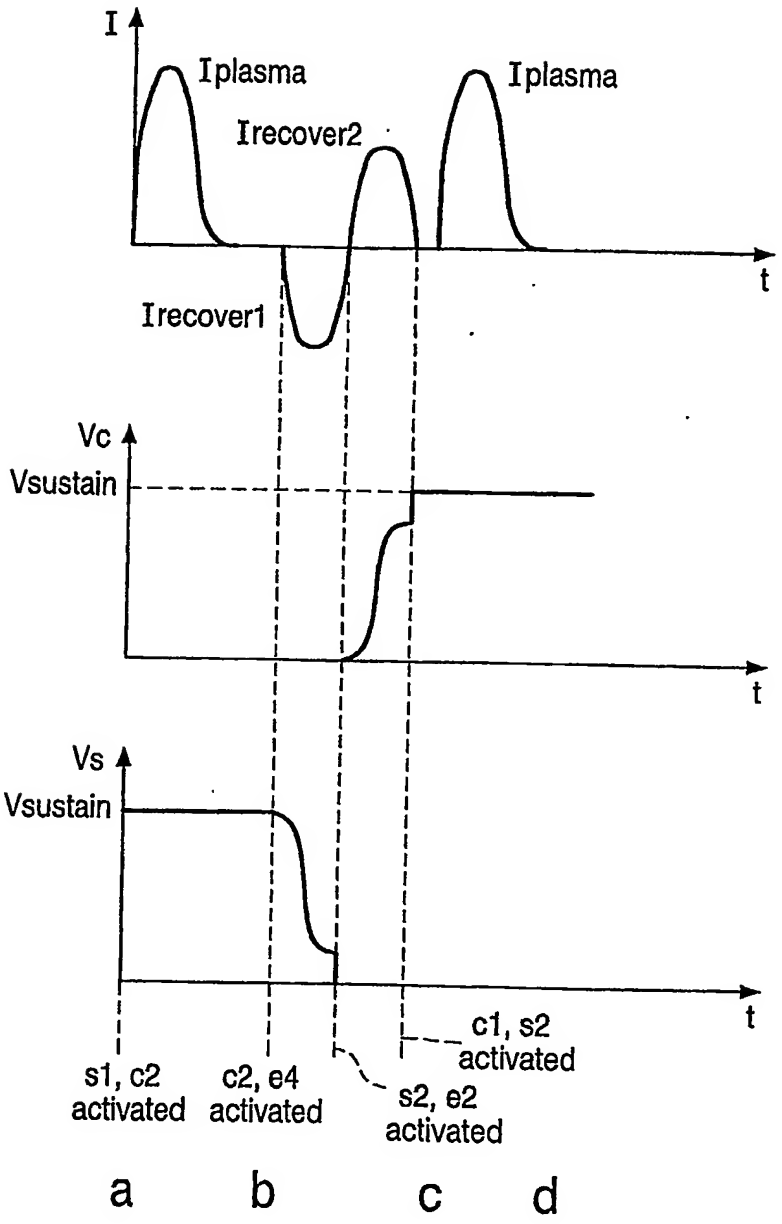
I
Iplasma
Irecover2
Iplasma
t
Irecover1
Vc
Vsustain
t
Vs
Vsustain
t
c1, s2
activated
s1, c2
activated
c2, e4
activated
s2, e2
activated
a
b
c
d

FIG. 6e

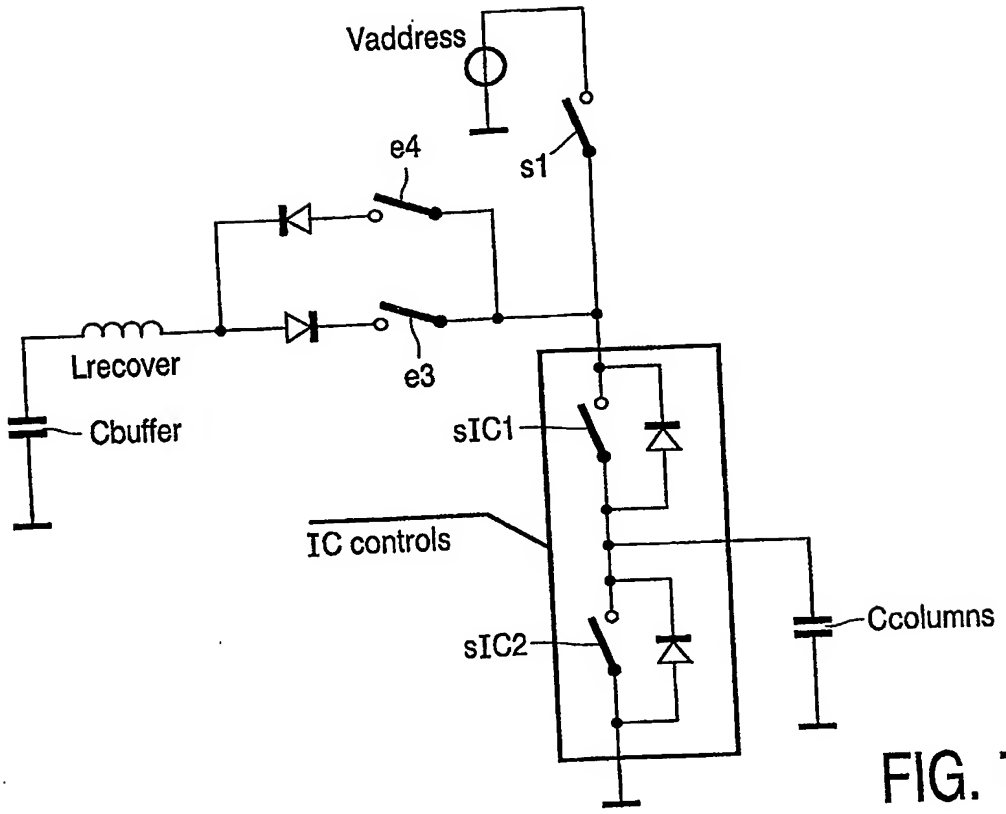
Vaddress
s1
e4
e3
Lrecover
Cbuffer
sIC1
IC controls
sIC2
Ccolumns

FIG. 7

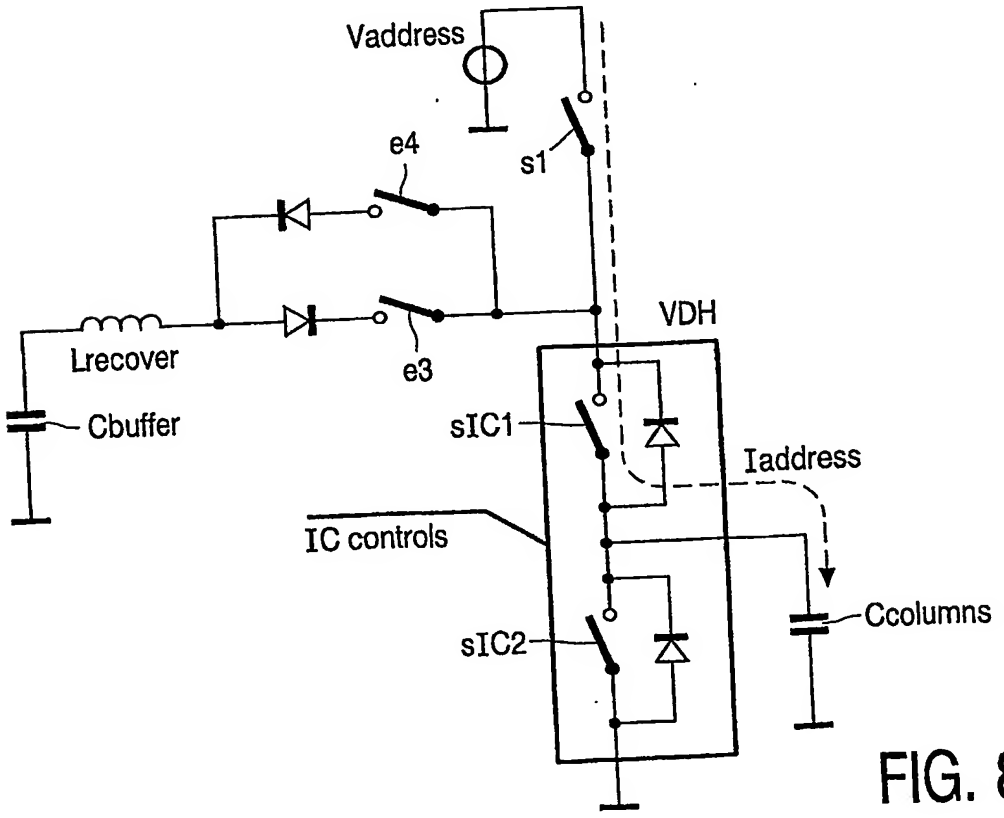
Vaddress
s1
e4
e3
VDH
Lrecover
Cbuffer
sIC1
Iaddress
IC controls
sIC2
Ccolumns

FIG. 8a

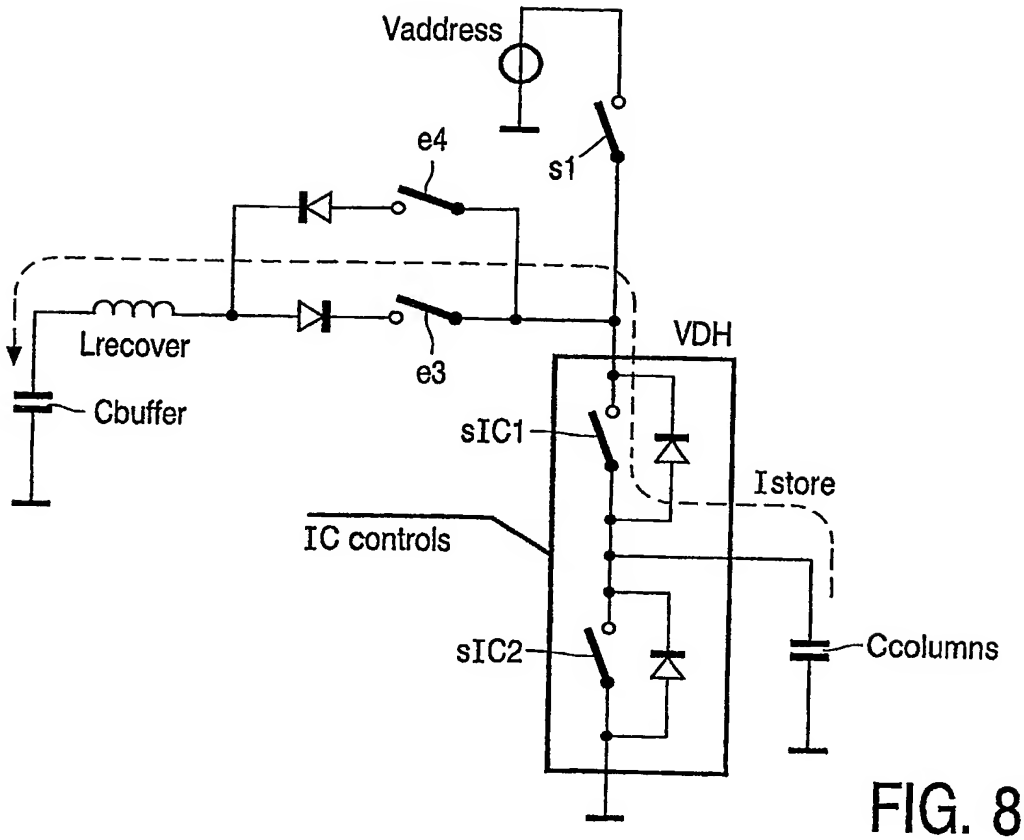
Vaddress
e4
s1
Lrecover
e3
VDH
Cbuffer
sIC1
Istore
IC controls
sIC2
Ccolumns

FIG. 8b

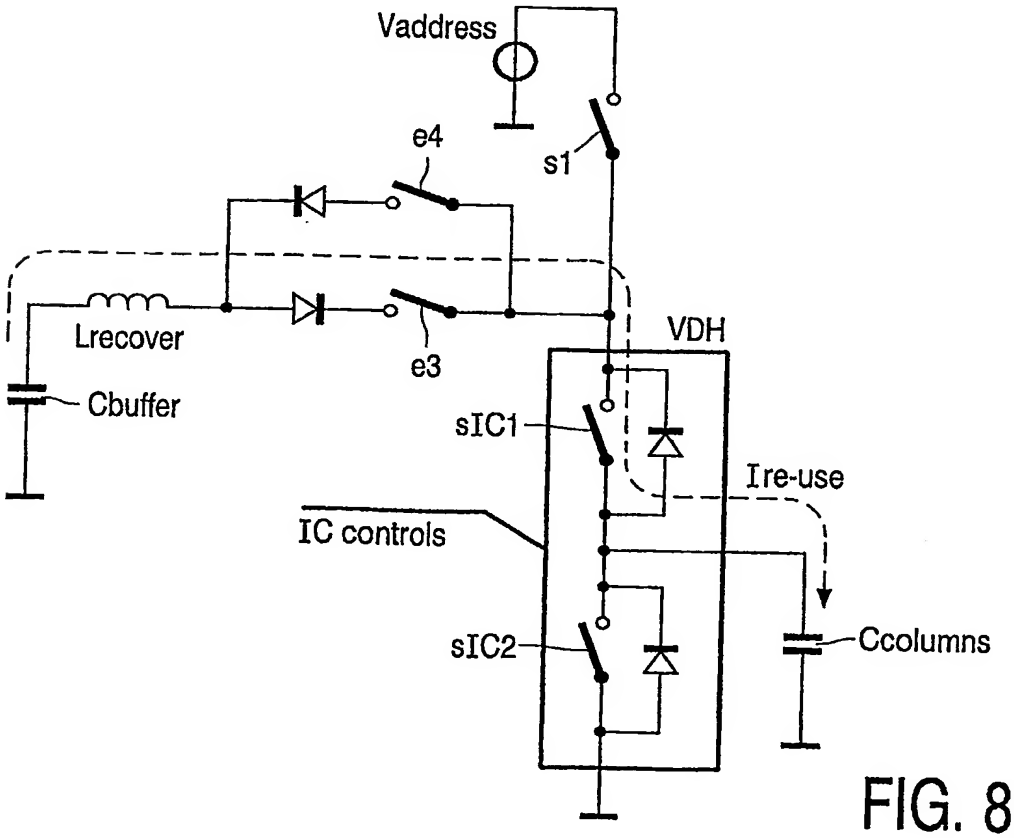
Vaddress
e4
s1
Lrecover
e3
VDH
Cbuffer
sIC1
Ire-use
IC controls
sIC2
Ccolumns

FIG. 8c

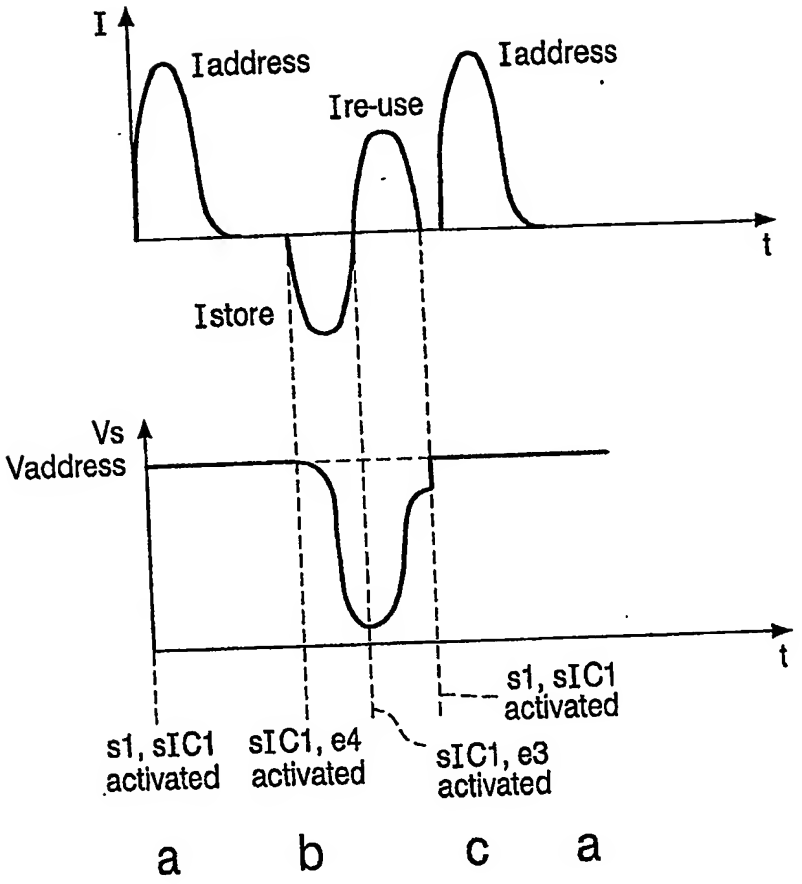
I
Iaddress
Ire-use
Iaddress
t
Istore
Vs
Vaddress
t
s1, sIC1
activated
s1, sIC1
activated
sIC1, e4
activated
sIC1, e3
activated
a
b
c
a

FIG. 8d

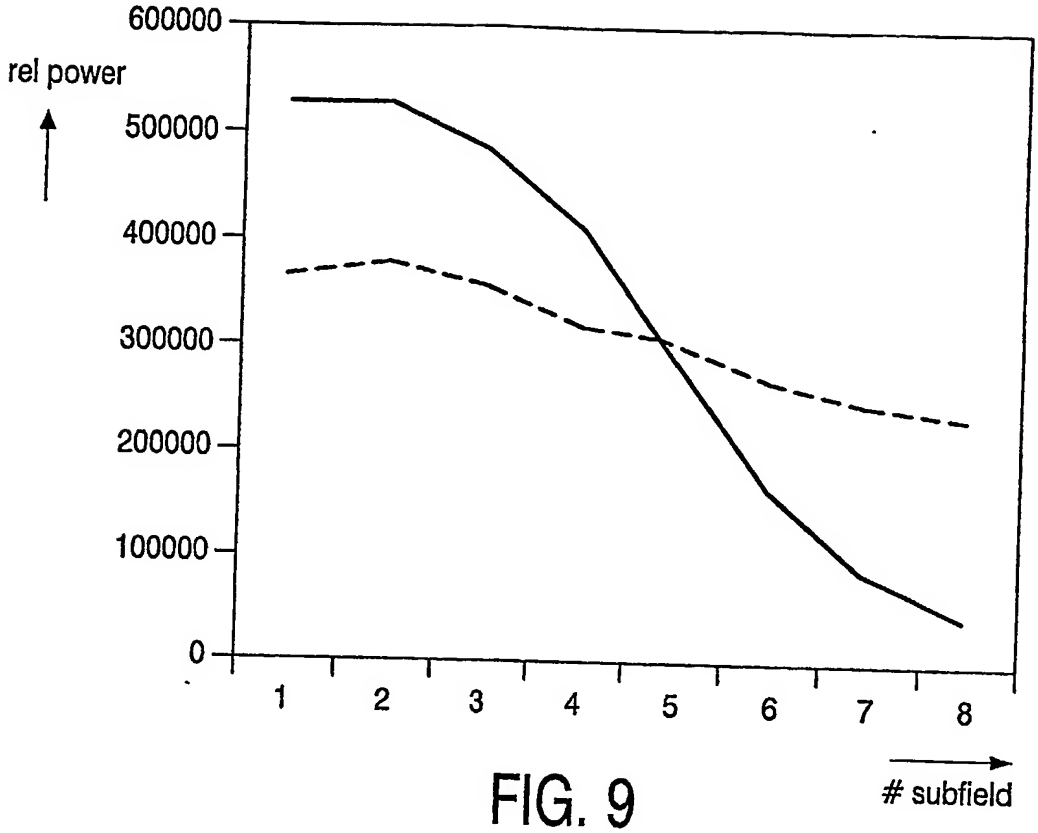
600000
rel power
500000
400000
300000
200000
100000
0
1
2
3
4
5
6
7
8
subfield

FIG. 9

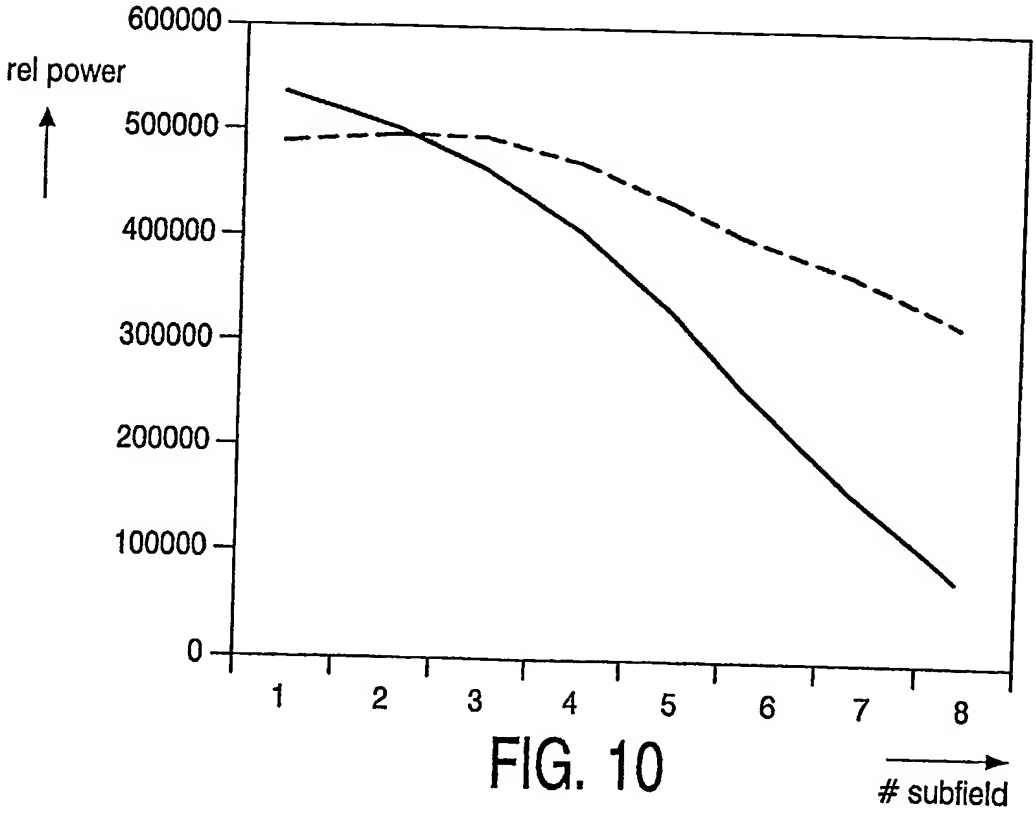
600000
rel power
500000
400000
300000
200000
100000
0
1
2
3
4
5
6
7
8
subfield

FIG. 10